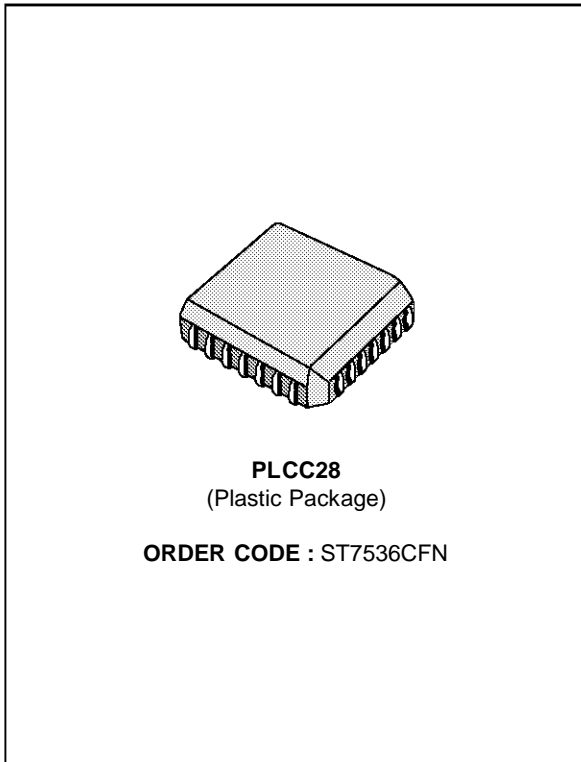


POWER LINE MODEM

- HALF DUPLEX SYNCHRONOUS FSK MODEM
 - Two programmable channels for 600bps data rate
 - Two programmable channels for 1200bps data rate
- AUTOMATICALLY TUNED Rx AND Tx FILTERS
- TX CARRIER FREQUENCIES SYNTHESIZED FROM EXTERNAL CRYSTAL
- LOW DISTORTION Tx SIGNAL ($S/H2 \geq 50\text{dB}$)
- AUTOMATIC LEVEL CONTROL ON Tx SIGNAL
- Rx SENSITIVITY: 2mV_{RMS} (600bps)
 3mV_{RMS} (1200bps)
- Rx CLOCK RECOVERY
- POWER-DOWN MODE
- SUITABLE TO APPLICATION IN ACCORDANCE WITH DH028/29 ENEL, EN50065-1 CENELEC AND FCC SPECIFICATIONS

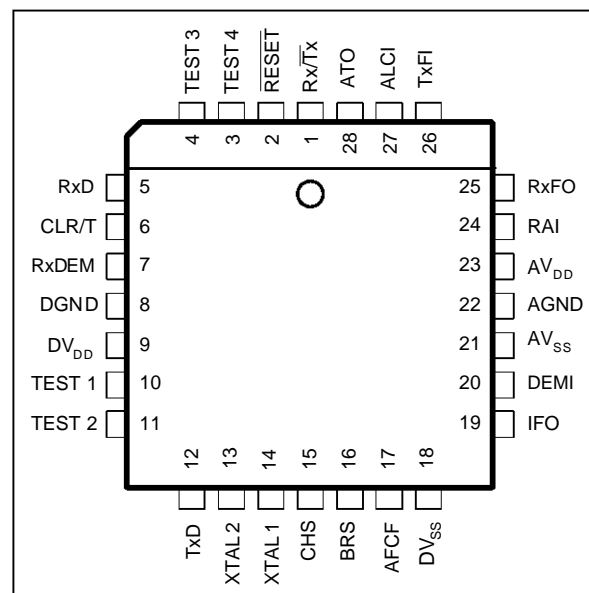


DESCRIPTION

The ST7536 is a half duplex synchronous FSK MODEM designed for power line communication network applications.

It operates from a dual power supply +5V and -5V, and requires an external interface for the coupling to the power line. It offers two programmable data rate with two programmable channels each.

PIN CONNECTIONS



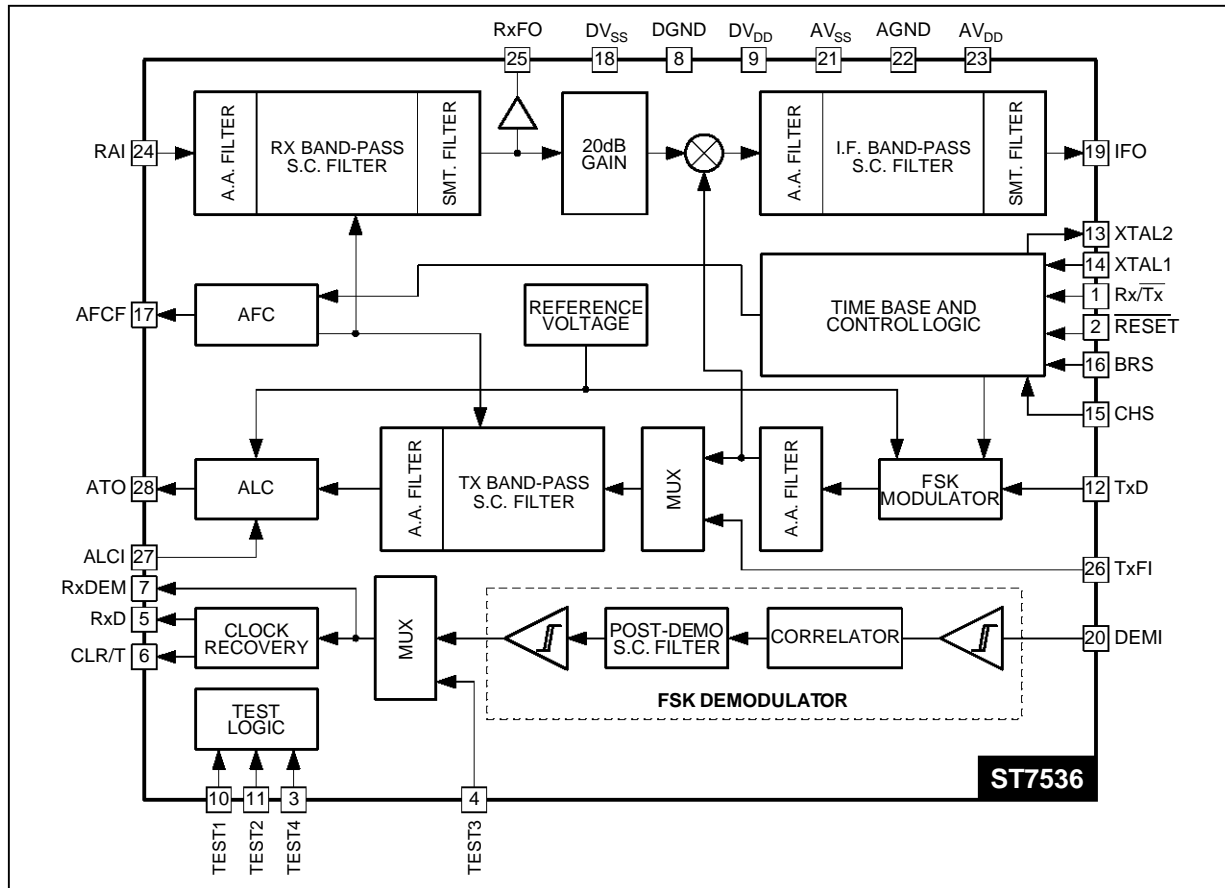
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PIN DESCRIPTION

Pin Name	Pin Number	Pin Type	Description
$\overline{\text{Rx/Tx}}$	1	Digital	Rx or Tx mode selection input
$\overline{\text{RESET}}$	2	Digital	Logic reset and power-down mode input. Active when low.
TEST4	3	Digital	Test input which selects the Tx band-pass filter input (TxFI) when high.
TEST3	4	Digital	Test input which gives an access to the clock recovery input stage. This input is selected when TEST1 is high.
RxD	5	Digital	Synchronous receive data output
CLR/T	6	Digital	Rx or Tx clock according to the functional mode
RxD _{EM}	7	Digital	Demodulated data output
DGND	8	Supply	Digital ground
DVDD	9	Supply	Digital positive supply voltage : $5V \pm 5\%$
TEST1	10	Digital	Test input which cancels the Tx to Rx mode automatic switching and validates TEST3 input. Active when high.
TEST2	11	Digital	Test input which reduces the Tx to Rx mode automatic switching time. Active when high.
TxD	12	Digital	Transmit data input
XTAL2	13	Digital	Crystal oscillator output
XTAL1	14	Digital	Crystal oscillator input
CHS	15	Digital	Channel selection input
BRS	16	Digital	Baud rate selection input
AFCF	17	Analog	Automatic frequency control output for connecting compensation network.
DVSS	18	Supply	Digital negative supply voltage : $-5V \pm 5\%$
IFO	19	Analog	Intermediate frequency filter output
DEMI	20	Analog	FSK demodulator input
AVSS	21	Supply	Analog negative supply voltage : $-5V \pm 5\%$
AGND	22	Supply	Analog ground : 0V
AVDD	23	Supply	Analog positive supply voltage : $5V \pm 5\%$
RAI	24	Analog	Receive analog input
RxFO	25	Analog	Receive filter output
TxFI	26	Analog	Transmit filter input (selected when TEST4 is high)
ALCI	27	Analog	Automatic level control input
ATO	28	Analog	Analog transmit output

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BLOCK DIAGRAM



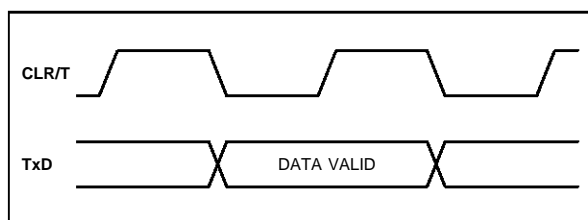
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TRANSMIT SECTION

The transmit mode is set when $Rx/\overline{Tx} = 0$, if Rx/\overline{Tx} is held at 0 longer than 3 seconds, then the device switches automatically in the Rx mode. A new activation of the Tx mode requires Rx/\overline{Tx} to be returned to 1 for a minimum 2 microsecond period before being set to 0.

The Transmit Data (TxD) is sampled on a positive edge of CLR/T which delivers the transmit bit clock when the transmit mode is selected. This data enters a FSK modulator whose two basic frequencies are selected by the Baud Rate Selection pin (BRS) and the Channel Selection pin (CHS) according to the Table 1.

Figure 1 : Tx Data Input Timing



7536-03.EPS

Table 1

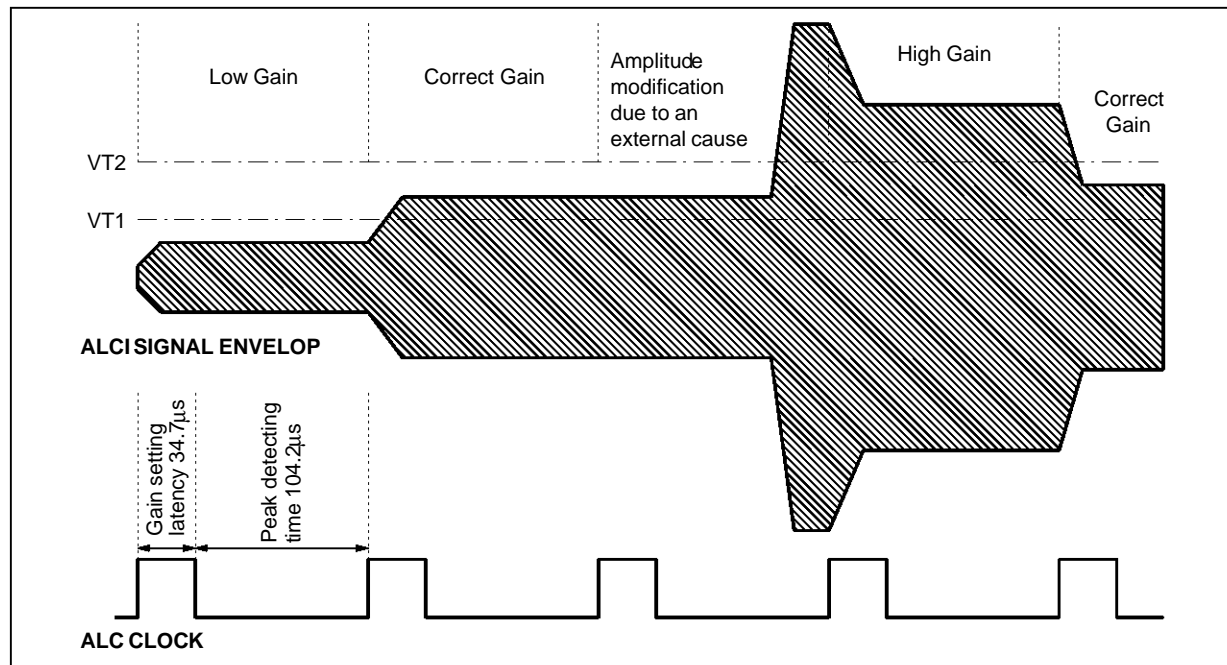
BRS	CHS	Baud Rate (Baud)	Tx Frequencies (kHz) TxD=1 - TxD=0
0	0	600	81.75 - 82.35
0	1	600	67.2 - 67.8
1	0	1200	71.4 - 72.6
1	1	1200	85.95 - 87.15

These frequencies are synthesized from a 11.0592MHz crystal oscillator ; their precision is the same as the crystal one's (100 ppm).

The modulated signal coming out of the FSK modulator is filtered by a switched-capacitor band-pass filter (Tx band-pass) in order to limit the output spectrum and to reduce the level of harmonic components.

The output stage of the Tx path consists of an Automatic Level Control (ALC) system which keeps the output signal (ATO) amplitude independent of the line impedance variations. This ALC is a variable gain system (with 32 discrete values) controlled by an analog feed-back signal ALCI (see Figure 2).

Figure 2 : Automatic Level Control Timing Chart



The ALC gain range is 0dB to -26dB and gain change is clocked at 7200Hz. Gain steps are of magnitude 0.84dB typically.

A period of this clock is decomposed into a 34.7µs gain settling latency and a 104.2µs peak detecting time. The gain change is related to the result of a peak detection obtained by making a direct comparison of ALCI maximum value (during detecting time) with two threshold voltages V_{T1} and V_{T2} (see Figure 2).

- $\max(\text{VALCI}) < V_{T1}$ - The next gain is increased by 0.84dB
- $V_{T1} \leq \max(\text{VALCI}) \leq V_{T2}$ - No gain change
- $V_{T2} < \max(\text{VALCI})$ - The next gain is decreased by 0.84dB.

RECEIVE SECTION

The receive section is active when $\overline{\text{Rx/Tx}} = 1$.

The baud rate and channel selection is also made according to Table 1.

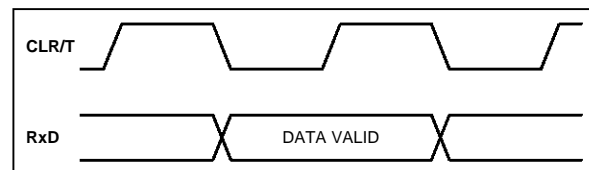
The Rx signal is applied on RAI with a common mode voltage of 0 volt and filtered by a band-pass switched capacitor filter (Rx band-pass) centered on the received carrier frequency and whose bandwidth is around 6 kHz. The input voltage range on RAI is $2\text{mV}_{\text{RMS}} - 2\text{V}_{\text{RMS}}$.

The Rx filter output is amplified by a 20dB gain stage which provides symmetrical limitations for large voltage. The resulting signal is down-con-

verted by a mixer which receives a local oscillator synthesized by the FSK modulator block. Finally an intermediate frequency band-pass filter (IF band-pass) whose central frequency is 2.7kHz when $\text{BRS} = 0$ and 5.4kHz when $\text{BRS} = 1$ improves the signal to noise ratio before entering the FSK demodulator. The coupling of the intermediate frequency filter output (IFO) to the FSK demodulator input (DEMI) is made by an external capacitor C5 ($1\mu\text{F} \pm 10\%$, 10V) which cancels the Rx path offset voltage.

A clock recovery circuit extracts the receive clock (CLR/T) from the demodulated output (RxDEM) and delivers synchronous data (Rx D) on the positive edge of CLR/T.

Figure 3 : Rx Data Output Timing



ADDITIONAL DIGITAL AND ANALOG FUNCTIONS

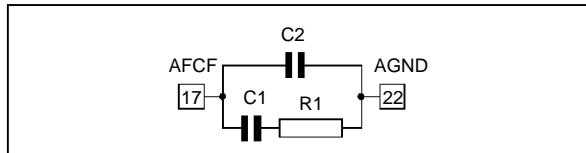
A reset input ($\overline{\text{RESET}}$) initializes the device.

When $\overline{\text{RESET}} = 0$, the device is in power-down mode and all the internal logic is reset. When $\overline{\text{RESET}} = 1$, the device is active.

A time base section delivers all the internal clocks from a crystal oscillator (11.0592MHz). The crystal is connected between XTAL1 and XTAL2 pins and needs two external capacitors C3 and C4 depending on the crystal characteristic typically 22pF ±10% for proper operation. It is also possible to provide directly the clock on pin XTAL1 ; in this case C3 and C4 should be removed.

An Automatic Frequency Control (AFC) Section adjusts the central frequency of Rx and Tx band-pass filter to the carrier central frequency. The stability of the AFC loop is ensured by an external compensation network C1 (470nF ±10%, 10V), C2 (47nF ±10%, 10V) and R1 (1.5kΩ ±5%) connected to pin AFCF.

Figure 4 : Automatic Frequency Loop Filter



7536-06.EPS

TESTING FEATURES

- An additional amplifier allows the observation of the Rx band-pass filter output on pin RxFO.
- A direct input to the Tx band-pass filter (TxFI) is available and selected when TEST4 = 1.
- The 3 second normal duration of the Tx to Rx mode automatic switching is reduced to 1.48ms when TEST2 = 1.
- When TEST1 = 1 the Tx to Rx mode automatic switching is deactivated and the functional mode of the circuit is controlled by Rx/Tx as

follow : when $Rx/Tx = 0$ the circuit is transmitting continuously, when $Rx/Tx = 1$ the clock recovery block is disconnected from the FSK demodulator for testing purpose, in this configuration TEST 3 is the data input of the clock recovery block, RXDEM follow TEST3 and Rx/D delivers the resynchronized data.

POWER SUPPLIES WIRING AND DECOUPLING PRECAUTIONS

The ST7536 has two positive power supply pins, two negative power supply pins and two ground pins in order to separate internal analog and digital supplies. The analog and digital terminals of each supply pair must be connected together externally and require special routing precautions in order to get the best receive sensitivity performances. The three major routing requirements are :

- The ground impedance should be as low as possible, for this purpose the AGND and DGND terminals can be connected via a local plane.
- The positive and negative power supplies (AV_{DD}, DV_{DD}, AV_{SS}, DV_{SS}) should be star-connected, avoiding common current path for the digital and analog power supplies terminals.
- Five decoupling capacitors located as close as possible to the power supply terminals should be used. Two 2.2µF tantalum and two 100nF ceramic capacitors perform the main decoupling function in the vicinity of the analog power supplies and a 100nF ceramic capacitor in the vicinity of the positive digital power supply is used to reduce the high frequency perturbations generated by the logic part of the circuit.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
AV _{DD} /DV _{DD}	Positive Supply Voltage (1)	-0.3, +7	V
AV _{SS} /DV _{SS}	Negative Supply Voltage (1)	-7, +0.3	V
V _{AGND} /DGND	Voltage between AGND and DGND	-0.3, +0.3	V
V _I	Digital Input Voltage	DGND-0.3, DV _{DD} +0.3	V
V _O	Digital Output Voltage	DGND-0.3, DV _{DD} +0.3	V
I _O	Digital Output Current	-5, +5	mA
V _i	Analog Input Voltage	AV _{SS} -0.3, AV _{DD} +0.3	V
V _o	Analog Output Voltage	AV _{SS} -0.3, AV _{DD} +0.3	V
I _o	Analog Output Current	-5, +5	mA
P _D	Power Dissipation	500	mW
T _{oper}	Operating Temperature	- 25, + 70	°C
T _{stg}	Storage Temperature	- 65, + 150	°C

7536-02.TBL

- Notes :**
1. The voltages are referenced to AGND and DGND.
 2. Latch-up problems can be overcome with 2 reverse biased schottky diodes connected respectively between A/DV_{DD} & A/DGND and A/DV_{SS} & A/DGND.
 3. Absolute maximum ratings are values beyond which damage to device may occur. Functional operation under these conditions is not implied.

GENERAL ELECTRICAL CHARACTERISTICS

The test conditions are A/DV_{DD} = +5V, A/DV_{SS} = -5V, A/DGND = 0V,
T_{amb} = -10 to 70°C unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ	Max	Unit
AV _{DD} /DV _{DD}	Positive Supply Voltage		4.75	5	5.25	V
AV _{SS} /DV _{SS}	Negative Supply Voltage		-5.25	-5	-4.75	V
AI _{DD} + DI _{DD}	Positive Supply Current in Tx Mode	$\overline{\text{RESET}} = 1, \overline{\text{RX/TX}} = 0$		30	35	mA
AI _{DD} + DI _{DD}	Positive Supply Current in Rx Mode	$\overline{\text{RESET}} = 1, \overline{\text{RX/TX}} = 1$		29	34	mA
AI _{SS} + DI _{SS}	Negative Supply Current in Tx Mode	$\overline{\text{RESET}} = 1, \overline{\text{RX/TX}} = 0$	- 34	- 29		mA
AI _{SS} + DI _{SS}	Negative Supply Current in Rx Mode	$\overline{\text{RESET}} = 1, \overline{\text{RX/TX}} = 1$	- 33	- 28		mA
AI _{DD} + DI _{DD}	Positive Power-down Current	$\overline{\text{RESET}} = 0, \overline{\text{RX/TX}} = 1$ XTAL1 = 1			1.2	mA
AI _{SS} + DI _{SS}	Negative Power-down Current		- 1.2			mA
V _{IH}	High Level Input Voltage	Digital inputs except XTAL1	2.2			V
V _{IL}	Low Level Input Voltage	Digital inputs			0.8	V
V _{OH}	High Level Output Voltage	Digital outputs, I _{OH} = - 400μA	2.4			V
V _{OL}	Low Level Output Voltage	Digital outputs, I _{OL} = 1.6mA			0.4	V
V _{IH}	High Level Input Voltage	XTAL1 input	3.6			V
DC	XTAL1 Clock Duty Cycle	External clock	40		60	%

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TRANSMITTER ELECTRICAL CHARACTERISTICS

The test conditions are A/DV_{DD} = +5V, A/DGND = 0V, A/DV_{SS} = -5V,
T_{amb} = -10 to +70°C unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ	Max	Unit
V _{TAC}	Max Carrier Output AC Voltage	R _L = 2kΩ, V _{ALCI} < V _{T1}	2.8	3.2	3.7	V _{PP}
HD2	Second Harmonic Distortion	R _L = 2kΩ, V _{ALCI} < V _{T1}			0.32	%
FD	FSK Peak-to-peak Deviation	BRS = 0 BRS = 1		600 1200		Hz Hz
TRxTx	Carrier Activation Time	After $\overline{\text{RX/TX}} 1 \rightarrow 0$ transition			1	ms
TALC	Carrier Stabilisation Time	ALC maximum settling time 32 gain steps			5	ms
DRNG	ALC Dynamic Range		25	26	27	dB
VT1	ALC Low Threshold Voltage		1.81	1.87		V
VT2	ALC High Threshold Voltage			2.12	2.18	V
GST	ALC Gain Step			0.84		dB
PSRR1 PSRR2	Power supply rejection ratio on ATO (1)	V _{IN} = 200mV _{PP} , f _{IN} = 50Hz on V _{DD} or V _{SS}	35 10			dB dB

7536-04.TBL

Note 1 : This characteristic is guaranteed by correlation.

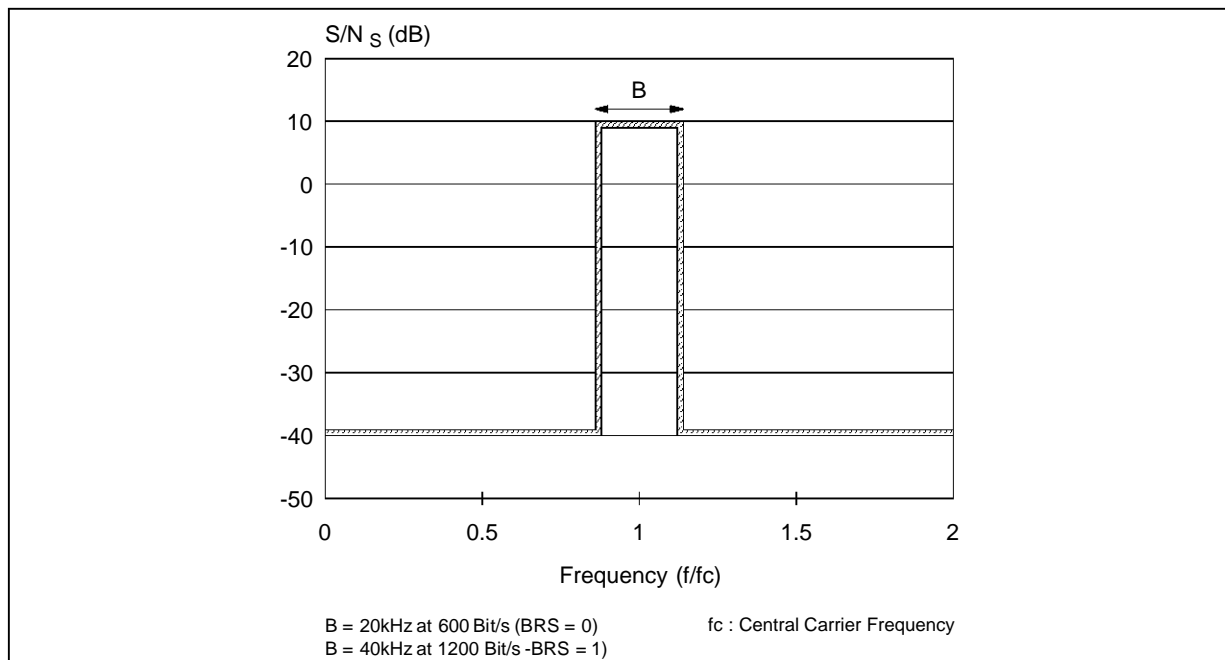
RECEIVER ELECTRICAL CHARACTERISTICS

The test conditions are A/DV_{DD} = +5V, A/DGND = 0V, A/DV_{SS} = -5V,
T_{amb} = -10 to +70°C unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _{IN}	Maximum Input Signal				2	V _{RMS}
R _{IN}	Input Impedance		100			kΩ
RCJ	Recovered Clock Jitter	Percentage of the nominal clock	- 5		+ 5	%
PSRR1 PSRR2	Power supply rejection ratio on RxFO (1)	V _{IN} = 200mV _{PP} , f _{IN} = 50Hz on V _{DD} or V _{SS}	35 10			dB dB
V _{IN0} V _{IN1}	Rx sensitivity (1)	Typical measured BER < 10 ⁻⁵ BRS = 0 BRS = 1			2 3	mV _{RMS}
BER1 BER2	Bit error rate at minimum Rx signal (1)	White Noise, S/N = 15dB RAI = 2mV _{RMS} , BRS = 0 RAI = 3mV _{RMS} , BRS = 1		2 · 10 ⁻⁵ 3 · 10 ⁻⁴	10 ⁻³ 10 ⁻³	
BER3	Bit error rate at maximum Rx signal (1)	RAI = 2V _{RMS} , White Noise S/N = 25dB		10 ⁻⁷	10 ⁻³	
BER4	Bit error rate at medium Rx signal (1)	RAI = 0.6V _{RMS} , S/N = 15dB		10 ⁻⁶	10 ⁻³	
BER5	Bit error rate with impulsive noise (1)	RAI = 90mV _{RMS} , N = 5V _{PP} pulse wave, f = 100Hz, duty cycle = 10%			10 ⁻³	
BER6 BER7	Bit error rate with modulated sinusoidal noise N _s (1)	S + N _s < 0.2V _{RMS} , N _s = sine carrier with 80% AM modul., f _m = 1kHz, See Figure 5 S _{min} = 2mV _{RMS} , BRS = 0 S _{min} = 3mV _{RMS} , BRS = 1			10 ⁻³ 10 ⁻³	

Note 1 : This characteristic is guaranteed by correlation

Figure 5 : S/N Mask for 80% AM Sine Noise

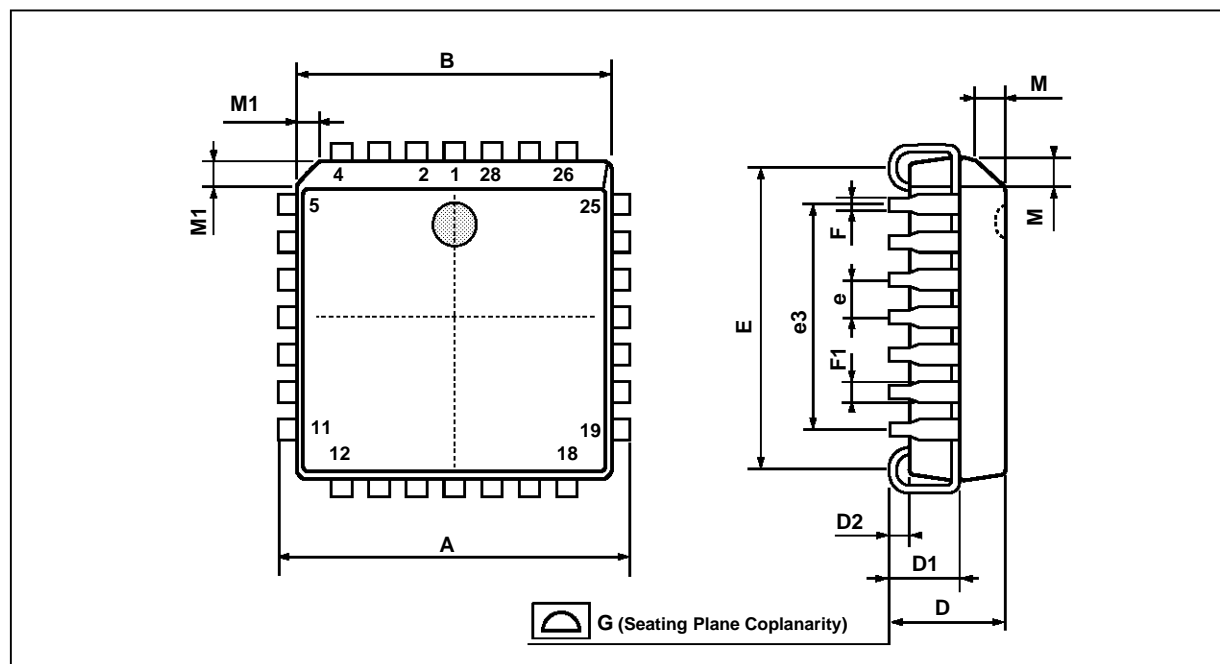


FILTER TEMPLATES

Frequency (kHz)	Test Conditions	Amplitude (dB)		
		Min.	Typ.	Max.
RECEIVE AND TRANSMIT FILTER				
54	BRS = 0, CHS = 0			- 35
79.05		- 4	- 3	- 2
Ref 82.05			0	
85.05		- 4	- 3	- 2
123				- 35
44.4	BRS = 0, CHS = 1			- 35
65		- 4	- 3	- 2
Ref 67.46			0	
69.93		- 4	- 3	- 2
101.13				- 35
47.57	BRS = 1, CHS = 0			- 35
69.64		- 4	- 3	- 2
Ref 72.28			0	
74.92		- 4	- 3	- 2
108.36				- 35
57.08	BRS = 1, CHS = 1			- 35
83.57		- 4	- 3	- 2
Ref 86.74			0	
89.91		- 4	- 3	- 2
130.03				- 35
INTERMEDIATE FREQUENCY FILTER				
1.2	BRS = 0			- 35
2.15		- 5	- 3	- 2
Ref 2.7			0	
3.25		- 5	- 3	- 2
5.8				- 35
2.4	BRS = 1			- 35
4.3		- 5	- 3	- 2
Ref 5.4			0	
6.5		- 5	- 3	- 2
11.6				- 35

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PACKAGE MECHANICAL DATA
28 PINS - PLASTIC CHIP CARRIER



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	12.32		12.57	0.485		0.495
B	11.43		11.58	0.450		0.456
D	4.2		4.57	0.165		0.180
D1	2.29		3.04	0.090		0.120
D2	0.51			0.020		
E	9.91		10.92	0.390		0.430
e		1.27			0.050	
e3		7.62			0.300	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.24			0.049	
M1		1.143			0.045	

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